A FULL-SWING 10-BIT CMOS CYCLIC DA CONVERTER WITH A CAPACITOR-SHARING TECHNIQUE FOR AUTOMATIC TEST EQUIPMENT

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Abstract - This paper describes a CMOS cyclic Digital-to-Analog Converter (DAC) for Automatic Test Equipment (ATE). In the middle of ATE, many kinds of DC reference voltages must be generated by DAC channels. In order to satisfy the DAC requirements, a small-area, a full-swing, and a high-resolution beyond 10-bit are needed. Therefore, a cyclic type DAC with a capacitor-sharing technique is proposed. Further, a full-swing output buffer is also discussed. The proposed DAC has been fabricated with 0.18um, 1-poly, and 5-metal CMOS process. The effective chip size is 0.28mm2 and the power dissipation is about 350uW at 5V power supply. The measured result of SFDR is 63dB, when the input frequency is 1MHz at the sampling frequency of 10MHz. The measured INL is within 1.5LSB and DNL is within 1.0LSB.

Index Terms - full-swing, cyclic DAC, capacitor-sharing technique, automatic test equipment (ATE)

I. INTRODUCTION

As the markets of semiconductor chipsarerapidly growing, the importance of chip test is also becoming bigger. In order to detect the defective chip products, an Automatic Test Equipment (ATE) is now widely used in the field of electronic manufacturing. Fig.1 shows a simple block diagram for a basic ATE. It is composed of a vector generator, a timing generator, a driver, an active load, a comparator, and a DC reference generator. Generally, there are three kinds of chip testing such as DC test, AC test, and function test. Firstly, the DC test measuresa static performance such as in/out voltages, currents, and operation voltages/currents. Secondly, the AC test measuresa dynamic performance such as transfer delay, set-up time, and hold time. Thirdly, the function test measuresthe interactions of each device cell. When the function test is chosen, a test vector generator show in Fig.1 is needed. After the generated vector is transferred into the timing generator and driver, the active load drives an optimized signal to the test chip. Then, the measured output of a test chip drives the comparator. Depending on the output of comparator, the judge block decides whether the test chip is perfective or not. To satisfy the various conditions above, ATE needs many kinds of DC reference voltages such as VIH, VIL, VOH, VOL, and so on. Those voltages are normally generated by a Digital-to-Analog Converter (DAC) shown in Fig.1. Further, since one reference voltage needs one DAC, many DACs are absolutely included in the middle of ATE. In the proposed ATE systems, at least 24 DAC channels are needed. Therefore, in order to satisfy the DAC requirements, a small-area, a full-swing, and a high-resolution beyond 10-bit must be designed.

There are many kinds of DAC such as decoder type, current steering type, cyclic type, and so on [1]-[14]. The decoder type is easily implemented by a simple digital block and an output buffer. However, the chip area is large, because it needs many MOS transistors. The most popular one in the field of DAC is the current steering type. It has the fastest operating speed and a high resolution beyond 12-bit. Even though the current steering type has an excellent performance, the chip area and power consumption are very huge. Above all, it has the critical drawbacks that it is almost impossible to have a full-swing. On the contrary, the cyclic type has a small-area, a full-swing, and a high-resolution, even though the operating speed is very slow [1][2]. Therefore, a CMOS cyclic DAC for ATE is discussed in this paper. The contents of the paper are as follows. In Section II,a simple principle of a cyclic DAC is described. In Section III, the circuit design and the proposed techniques are discussed. The experimental resultsare described in Section IV. Finally, the conclusion is summarizedin Section V.

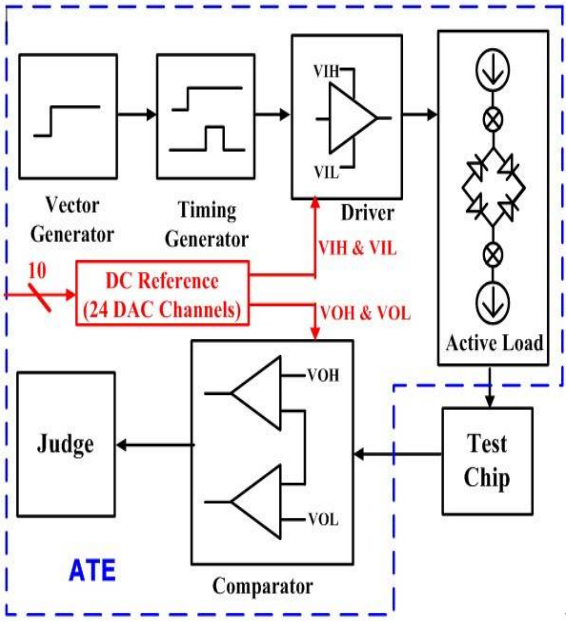


Fig. 1. Block diagram of an automatic test equipment

II. PRINCIPLE OF A CYCLIC DAC

Fig. 2 shows a basic structure of cyclic DAC [2][3]. It is composed of four switches and two capacitors. The operating principle is as follow. At first, the switch φ4 isturn-on to discharge Cy, and the initialization has been done. Then, depending onthe input digital code, the switch φ1 and φ2 are turn-on or turn-off. For example, assuming the input digital code is high, the switch φ1 is only turn-on and Cx is charged into V_{REF}. Assuming the input digital code is low, the switch φ2 is only turn-on and Cx is discharged into GND. Finally, the switch φ3 is only turn-on to make an average between Cx and Cy, before the next higher bit is starting. The order of digital code is starting from the LSB (Least Significant Bit) into the MSB (Most Significant Bit). Thesame operation is repeated until the end of digital input code. Thus the final output voltage at the end of n-th cycle for the cyclic DAC can be written as

$$\mathrm{Vo(n)} = \left(D_{n-1} \cdot V_{REF} + Vo(n-1)\right) \cdot \frac{1}{2} \qquad (1)$$

Where Vo(n-1) is the previous voltage of Cy, and the initial condition of Vo is zero. For example, assuming that the digital code is 101 for a 3-bit cyclic DAC, Fig. 3 shows the operation principle one by one. At first, at the LSB shown in Fig.3(a), Cx is charged into V_{REF}, and the output voltage is $(1/2)V_{REF}$ after the average operation is done. Secondly, at the middle bit shown in Fig.3(b), Cx is discharged to 0V, and the output voltage is $(1/4)V_{REF}$ after the average operation is done. Finally, at the MSB shown in Fig.3(c), Cx is charged into V_{REF}, and the output voltage is $(5/8)V_{REF}$after the average operation is done. Thus, the desired analog output voltage of $(5/8)V_{REF}$is obtained, when the digital input code is 101.

From the discussion above, therefore, a cyclic DAC has a disadvantage of very lowoperating speed, since the input digital code must be serially processed one by one. However, independent of digital code resolution, the cyclic DAC almost has the same chip area. Further, it is possible to have a full-swing output voltage and a low power consumption [2]. In case of ATE, the cyclic DAC is one of the best candidates, because ATE needs at least 24 DAC channels.

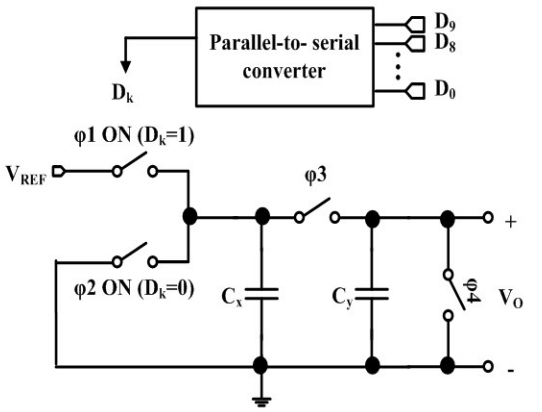


Fig. 2 Basic structure of a cyclic DAC

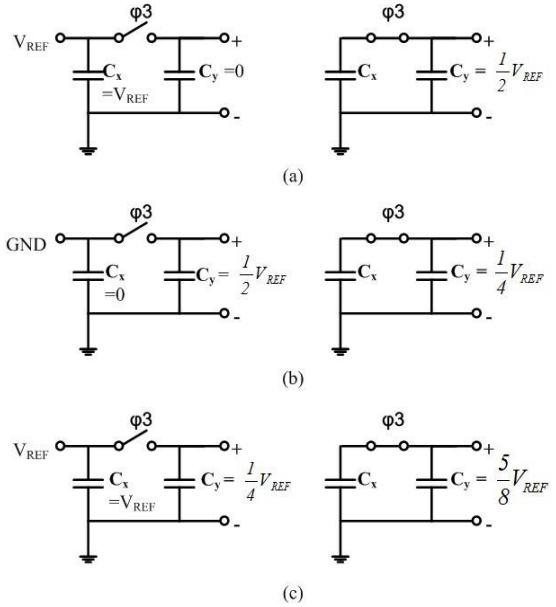


Fig. 3. Example of 3-bit cyclic DAC for 101 digital code (a) D_0=1 (LSB), (b) D_1=0 (Second bit), (c) D_2=1 (MSB).

III. CIRCUIT DESIGN

A. Architecture of the Proposed Cyclic DAC

Fig. 4 shows the full block diagram of the proposed cyclic DAC with a capacitor-sharing technique. It is composed of a digital block and an analog block. In the digital block, thereexistsa Johnson counter, a timing generator, a non-overlap clock generator, and a level shifter. Fig.5 shows the circuit diagram and operation principle of the 4-bit Johnson counter. It is a well-known circuit and easily understood. With the Johnson counter generated bythe main external clock,the timing generator makes various switch signals and convertsthe parallel digital codesinto the serial codes. Since most of the switches must not overlap each other, a non-overlapping clock generator accomplishes this function. Before the digital block drives the analog block, those digital signals have to be changed into a higher voltage by level shifter.This is because the power supply of digital block is 1.8V, while that of analog block is 5V.

Fig.6 shows the timing diagram for each clock. When the switch $\varphi_{in\ odd}$ turns on, the analog VDD or GND due to the input digital code is transferred into the input capacitor C_A. Then, the capacitor C_A and C_B are connected, when the switch φ_{avg} turns on. Thus the average analog voltage between C_A and C_B is obtained and it is stored at the capacitor C_B. After 10 clocks of $\varphi_{in\ odd}$ and $\varphi_{avg}$are driven, $\varphi_{hd\ odd}$ turns on and the desired analog voltage is stored at the capacitor C_{Hold} through an analog buffer. Finally, the output analog voltage is obtained at the second analog buffer.This procedure is repeated until the input digital code is over.In order to improve the switch performance, there are many switches and a capacitor-sharing technique is proposed. Further, a full-swing output analog

voltage is available. It is discussed in the next section.

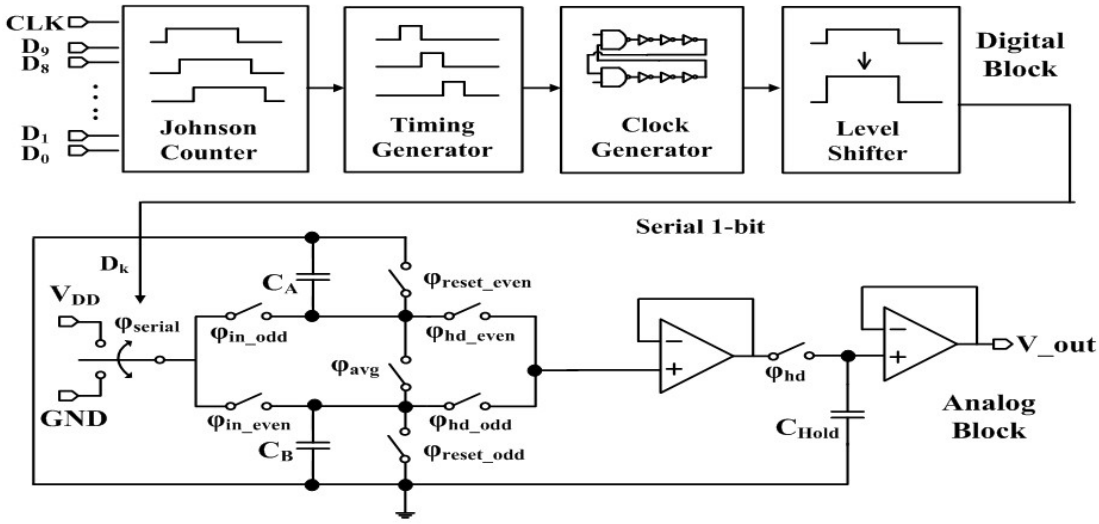


Fig. 4. Full block diagram of the proposed cyclic DAC with a capacitor-sharing technique

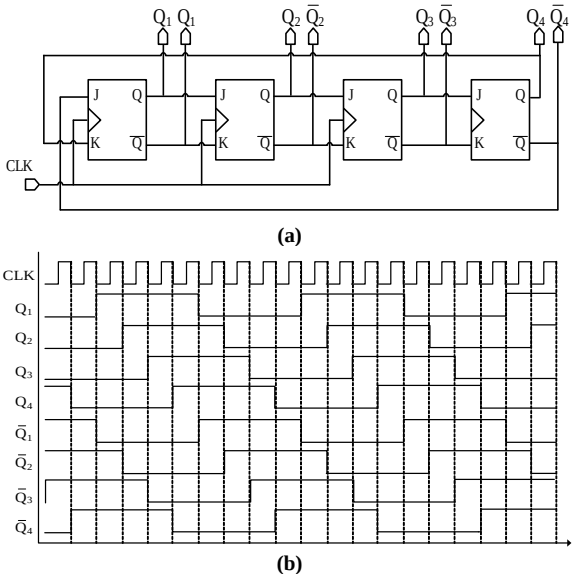


Fig. 5 (a) circuit diagram of the 4-bit Johnson counter (b) operation principle of the 4-bit Johnson counter.

Fig. 6. Timing diagram for each clock

B. A New Full-Swing Capacitor-Sharing Technique

The analog block shown in Fig.4 is composed of aninput analog multiplexer, nineswitches, three capacitors, and two analog buffers. Depending on the input digital code, the input sampling capacitor and the output holding capacitor are alternatively exchanged. Fig.7 shows the operation process of proposed DAC.When an odd digital code is driven as shown in Fig.7(a), C_A is sampling the input voltage by the switch φ_{in_odd}. At that time, C_B is holding the voltage of the previous state. Thus, the charge is redistributed between C_A and C_B, when the distribution switch $\varphi_{avg}$is ON. When an even digital code is driven as shown in Fig.7(b), C_B is sampling the input voltage by the switch $\varphi_{in_even}$and C_A is holding the previous voltage. In the same way, the charge is redistributed between C_B and C_A, when the distribution switch $\varphi_{avg}$is ON. Therefore, the role of capacitors is alternatively exchanged and the capacitors are sharing each other for odd digital codes and even digital codes. If the capacitor-sharing technique is used, the capacitor mismatching problems are drastically reduced. Furthermore, other side effects due to parasitic capacitances and switch errors are also decreased.

C. Calculation of Capacitor Value and Buffer Gain

In this structure, the decision of capacitor size is very important. Since a real capacitor has KT/C noise, the capacitor size to satisfy the specifications of n-bit DAC resolution is written as follows [12].

$$\frac{K \cdot T}{C_{min}} \leq \frac{V_{PP}}{2^n} \frac{K \cdot T}{V_{PP}} \cdot 2^n \leq C_{min} \qquad (2)$$

Here K is Boltzmann constant, T is room temperature, Vpp is the output analog voltage, and C_{min} is the minimum capacitor size which satisfies the n-bit DAC resolution. Based on the theory (2), the capacitor value is chosen as 500fF.

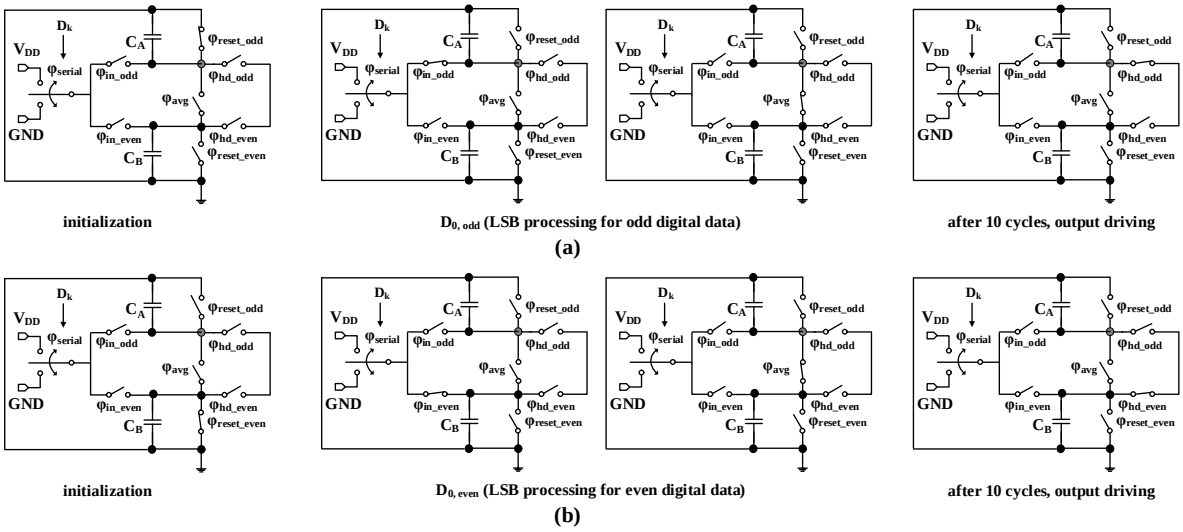


Fig.7. Operation process for the proposed capacitor-sharing technique (a)odd digital code (b)even digital code

In order to obtain a full-swing analog output voltage, a rail-to-rail operational amplifier is designed. Further, the open loop gain should be enough high. If the gain of operational amplifier is not enough high, some errors are occurred at the output buffer. The error of closed loop is expressed as follows.

$$\epsilon_0(\%) = \left(1 - \frac{A_O}{1 + A_O}\right) \times 100 \qquad (3)$$

In this equation (3), A_O is the open loop gain of operational amplifier. In order to reduce the errors within 0.1%, the open loop gain must be higher than 100dB.

IV. EXPERIMENTAL RESULTS

In order to verify the performance of the proposed cyclic DAC, a prototype 10-bit 10MS/s DAC has been fabricated with Magna 0.18um 5V CMOS process. Fig. 8(a) shows the total chip microphotograph with the proposed cyclic 10-bit DAC, and Fig. 8(b) shows themagnified layout for the DAC. The chip area is about 0.28mm^2 ,525um x 532um. The power consumption is about 350uW at the power supply voltage of 5.0V. A few decoupling capacitors are integrated into the chip at the spare spaces to reduce the interference among the individual blocks, EMI problems and power supply noise. Fig.9 shows a photograph for the printed circuit board withthe prototype chip. In order to measure the performance of DAC, compuscope 3200® is used to obtain many performances such as SFDR, INL, DNL,and so on. Fig.10 shows measurement results for INL, DNL and FFT spectrum of the proposed DAC at the sampling frequency of 10MS/s and input frequency of 1MHz. SNDR and SFDR are shown in FFT spectrum measurement results. The measured result of SFDR is about 63dB, INL is within +1.5LSB/-1.5LSB, and DNL is within +1.0LSB/-1.0LSB. Fig. 11 shows measured results for the full-swing output analog voltage. From 0V to 5V, a full-swing ramp is obtained.Fig.12 shows SFDR of the proposed cyclic DAC. The measured results are summarized in Tab.1. Tab.2 shows the performance comparison between the conventional ones and the proposed one.

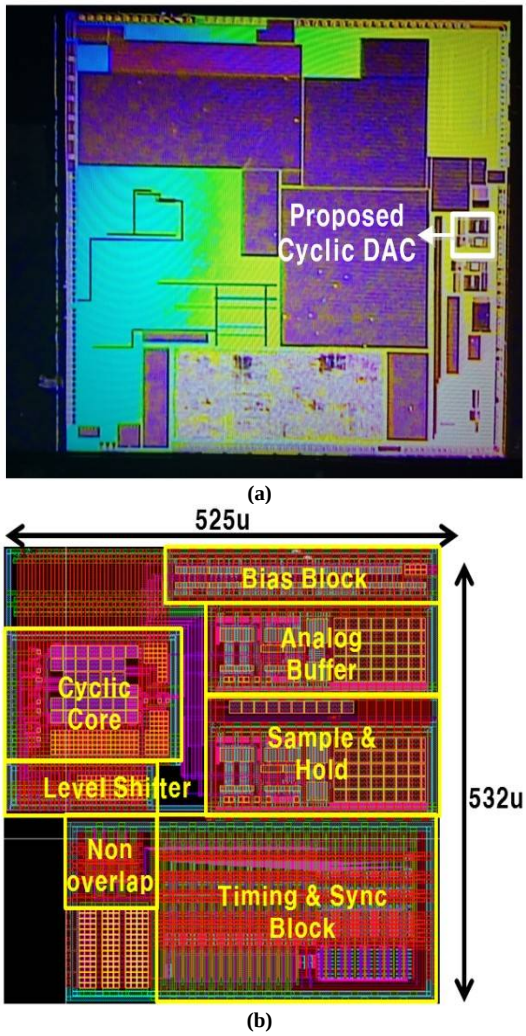


Fig. 8. (a) Microphotograph for the fabricated chip (b) Magnified layout for the proposed cyclic 10-bit DAC

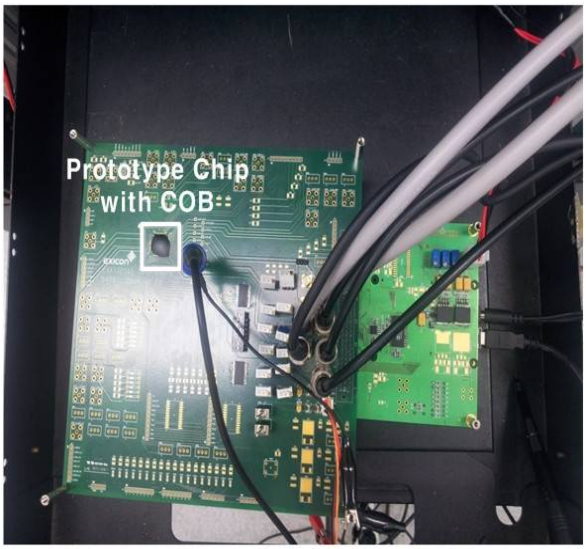


Fig. 9 Photograph for the test PCB with the fabricated chip

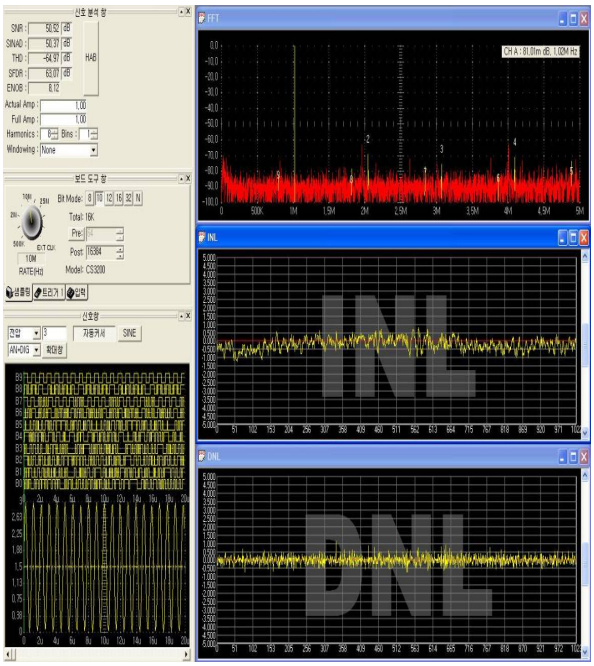


Fig. 10 Measured results for SFDR, INL, and DNL

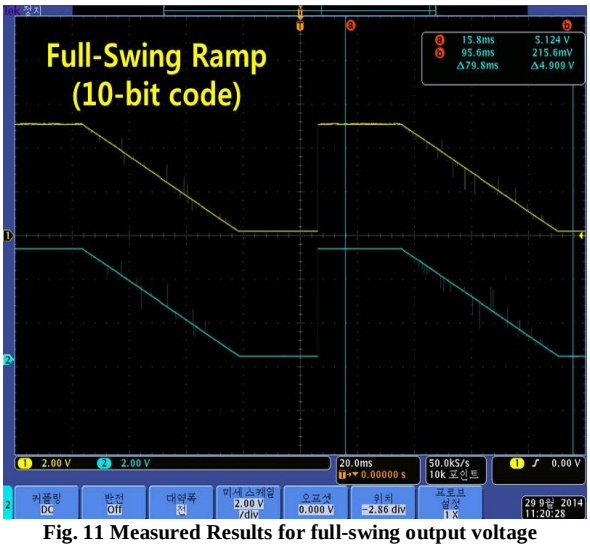


Fig. 11 Measured Results for full-swing output voltage

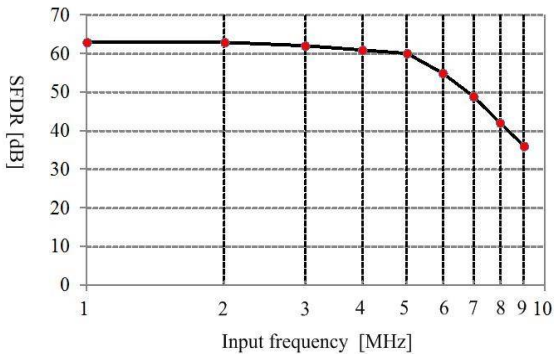


Fig. 12 Measured SFDR vs input frequency (@10MHz)

Table 1. Summary of measured results

Resolution	10-bit
Sampling Frequency	10MS/s
Power Supply	5.0V
Output Range	5.0 Vpeak Full Swing
SFDR (@10MSPS)	60dB (fin = 5MHz)
INL/DNL	±1.5LSB / ±1.0LSB
Power consumption	350μW
Core area	525μm x 532μm (0.28mm^2)
Technology	Magna 0.18μm CMOS

Table 2. Performance comparison

	[5]	[12]	This work
Resolution [bit]	10	10	10
CMOS Technology [um]	0.35	0.18	0.18
Sampling Rate [MS/s]	100	5	10
SFDR [dB]	65	62	60
INL/DNL [LSB]	0.5/0.5	1.0/1.0	1.5/1.0
Power Supply [V]	3	3	5.0
Output Swing [V]	1.2	1.2	5.0
Full Swing	No	No	Yes
Power Consumption [mW]	45	1	0.35
Chip Area [mm^2]	1.01	0.5	0.28
FoM [fJ/conv]	439	195	91

CONCLUSIONS

In this paper, a 10-bit CMOS cyclic DAC for automatic test equipment (ATE) was designed. In order to satisfy the DAC requirements for ATE, a small-area, a full-swing, and a high-resolution beyond 10-bit were needed. As well as anovel capacitor-sharing technique to reduce the mismatching errors wasproposed, a full-swing output buffer was also discussed. The proposed DAC has been fabricated with 0.18um, 1-poly, and 5-metal CMOS process. The effective chip size was 0.28mm^2 and the power dissipation was about 350uW at 5V power supply. The measured result of SFDR was 63dB, when the input frequency was 1MHz at the sampling frequency of 10MHz. The measured INL was within 1.5LSB and DNL was within 1.0LSB.

The FOM of this work is better than that of the conventional ones. Therefore, the proposed cyclic DAC is useful to satisfy the requirements of ATE.

ACKNOWLEDGMENTS

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