2-DIMENSIONAL ANALYSIS OF THE PARTIAL SOI TYPE ISOLATION MOSFET WITH DIFFERENT BURIED INSULATOR DIELECTRIC

[1]YOUNG KWON KIM, [2]MYOUNG JIN LEE, [3]JIN SUNG LEE, [4]GEON KIM

[1,2,3]School of Electronics and computer Engineering, Chonnam National University
E-mail: [1]yyong13@naver.com, [2]mjlee@chonnam.ac.kr, [3]lsc5176@naver.com, [4]rjsdlchd@naver.com

Abstract - As scaling down the DRAM cell size, the conventional MOSFET degrade device performance in terms of short channel effects. A solution for these issues is the Silicon-on-Insulator (SOI) MOSFET. However, it suffers from low threshold voltage, back gate interface issue, floating body effect such as kink effect, and high price, even though it shows low power consumption, self-limited shallow junction, improved Drain Induced Barrier Lowering (DIBL). To overcome the problem, a new device partial SOI type isolation MOSFET has been introduced [1]. The structure of this device is obtained by penetrating the insulator below the N type doped region near the drain region. And the lateral encroachment length of the buried insulator is controlled by isotropic etch time. This device can effectively improve short channel effects while improving the disadvantages of the conventional MOSFET and the SOI MOSFET. In the paper, the partial SOI type isolation MOSFET having 100nm node of gate channel length is investigated using Sentaurus TCAD 2-D device simulator [2]. And This study was conducted to investigate the performance of partial SOI type isolation MOSFETs according to the dielectric constant. The results show that the low-k dielectric of the buried insulator increases the threshold voltage and improves the DIBL characteristic due to decrease in the depletion region width near the drain region. Also, it is confirmed that the kink effect disappears unlike the SOI MOSFET due to the difference in structure.

Index Terms - Drain Induced Barrier Lowering (DIBL), Silicon-On -Insulator (SOI), Short Channel Effect (SCE)

I. INTRODUCTION

As the design rule of the DRAM cell decreases, it becomes very difficult to obtain sufficient data retention time. One of the main reasons is the decrease of V_{th} by Drain Induced Barrier Lowing(DIBL) and the increase of off-current by gate induced drain leakage (GIDL). To solve these problems, SOI MOSFET through the SOI process has appeared. In general, SOI MOSFET is known to have short channel effect smaller than that of a bulk MOSFET [3],[4]. Due to the structural characteristics of the SOI MOSFET, it has high integration and low parasitic capacitance due to isolation by an insulator [5]. But, despite the advantages such as low power consumption, self-limited shallow junction, and lower subthreshold slope(SS), SOI structures still suffer from low V_{th}, back gate interface problem, floating body effect and high price [6],[7]. A partial SOI type isolation MOSFET has been proposed to overcome this disadvantage of SOI MOSFET. It can be fabricated without using SOI process because the insulator is penetrated to a certain depth under the drain region of the MOSFET. Therefore, since the channel region is not fully depleted, the kink effect by the floating body effect, which is one of the biggest weaknesses of the SOI MOSFET, is structurally completely blocked. In addition, the short channel effect can be improved through the penetration effect of the insulator without decreasing the V_{th} in the low drain voltage state [8]. In this paper, we fabricated a partial SOI type isolation MOSFET with a gate channel length of 0.1 um using Sentaurus TCAD 2-D device simulator and analyzed the electrical characteristics according to the dielectric constant of the buried insulator. It is found that the width of the depletion region between the drain and channel changes due to the penetration of the buried insulator. We also confirmed on-current, DIBL, and V_{th} characteristics as the dielectric constant of the buried insulator.

II. DEVICE STRUCTURE

To study the buried insulator effect on the partial SOI type isolation MOSFET, a schematic cross-sectional view of the partial SOI type isolation MOSFET is simulated using Sentaurus TCAD 2-D device simulator. As shown the fig 1, The peak doping concentration of S/D region is kept at $1.2\times10^{-19}cm^{-3}$ and Peak channel doping concentration is kept $9\times10^{-17}cm^{-3}$. The analyzed partial SOI type isolation MOSFET has a gate channel length of 100nm and the gate channel length for Fig 1 is only 200nm. The gate oxide thickness, The S/D junction depth, and buried insulator thickness are 6nm, 110nm, 210nm respectively. We assumed metal gate workfunction of 4.17eV in the paper. The planar MOSFET and the SOI MOSFET in this paper is benchmarked with the same parameters using Sentaurus TCAD 2-D device simulator. The buried insulators of different dielectric constant were used, including SiO_2(k=3.9), Si_3N_4(k=7.5), HfO_2(k=25) to investigate the change of depletion region width near the drain region on the

partial SOI type isolation MOSFET. For the reliable simulation, the mobility model based on the drift-diffusion model and mobility saturation model in the high electric field are considered. These models were applied to the sdevice provided by the Sentaurus TCAD 2-D device simulator.

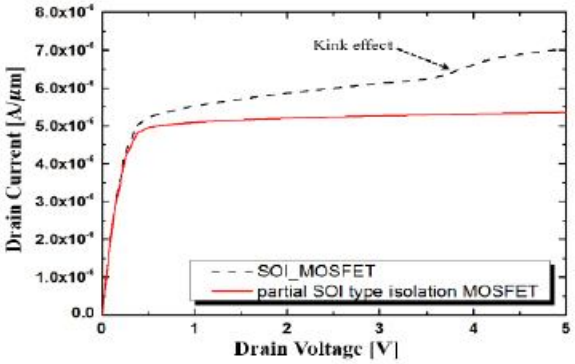


Fig 1. Ids-Vds characteristic for SOI MOSFET and partial SOI type isolation MOSFET at Vgs=1.2V. The silicon film thickness of SOI MOSFET and partial SOI type is 30nm respectively.

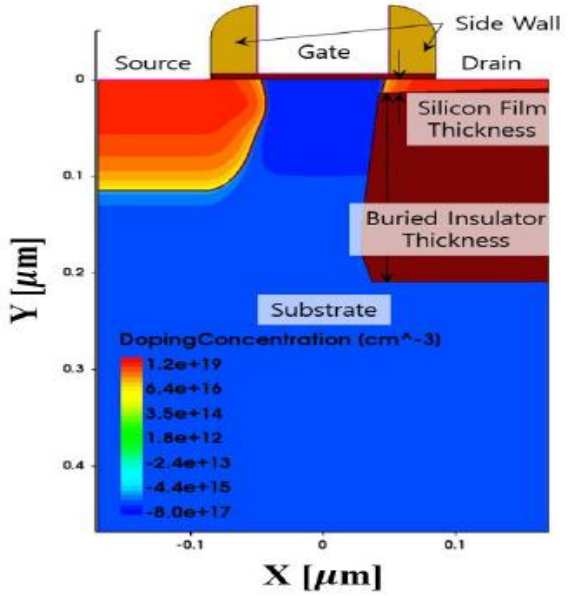
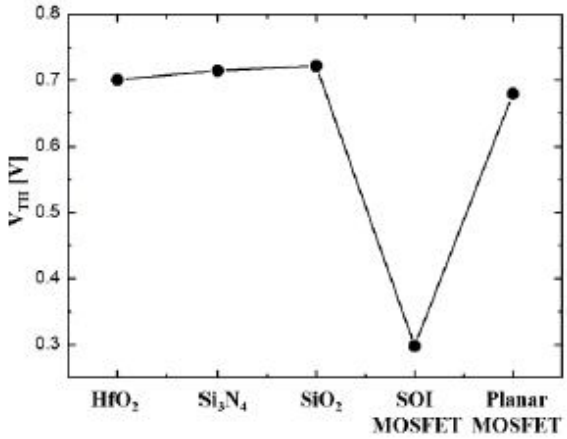


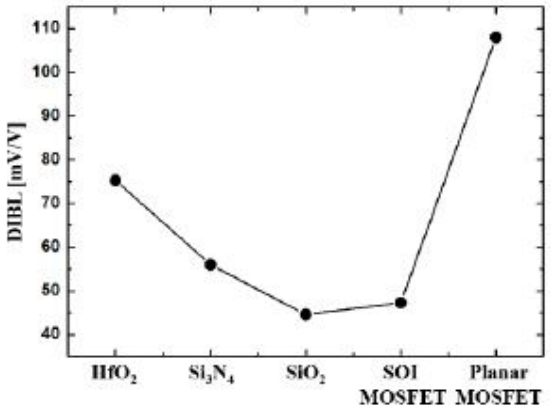
Fig 2. Illustration of simulated structure of partial SOI type isolation MOSFET

III. SIMULATION RESULTS AND DISCUSSION

First, Partial SOI type isolation MOSFETs do not have a kink effect, which is one of the disadvantages of SOI MOSFETs, because the channel is not fully depleted. As shown in Figure 2, the SOI MOSFET generates the kink effect near V_{ds}=4V while the partial SOI type isolation MOSFET remains saturated current [9]. Fig. 3 (a) and (b) respectively shows the V_{th} and DIBL of the partial SOI type-isolation MOSFETs. It is shown that the threshold voltage of the partial SOI type isolation MOSFET having buried insulator material of SiO_2(k=3.9) is the highest, while the threshold voltage of the SOI MOSFET is the lowest. The DIBL characteristics were excellent for the partial SOI type isolation MOSFET having buried insulator material of SiO_2(k=3.9). The DIBL is estimated based on the conventional equation, $(V_{th,lin}-V_{th,sat})$ / $(V_{d,sat}-V_{d,lin})$, where the constant current(~10^{-7}A/um) method is used for $V_{th,\,lin}$ and $V_{th,sat}$. In order to understand the physical details of V_{th} and DIBL improvement in the partial SOI type isolation MOSFET, device simulations have performed using Sentaurus tool as shown Fig. 4. The improvement of DIBL depends on the magnitude of the electric field penetrated to the source. As shown in Fig. 4 (a), when a high voltage is applied to the drain, the planar MOSFET forms a wide depletion region between the drain and the substrate. This means that the electric field at the drain is well transferred to the source. However, Fig. 4 (b) shows significantly smaller depletion region width than the planar MOSFET due to the large electric field near the drain region by the buried insulator having low dielectric constant. Namely, this means that a small electric field penetrates the source junction. Fig. 4 (c) shows the depletion layer width of a partial SOI type isolation MOSFET with k = 25. A partial SOI type isolation MOSFET with a large permittivity has a wide depletion layer width between the drain and the substrate.



(a)



(b)

Fig 3. (a), (b) Simulation result for threshold voltage and DIBL for planar MOSFET, SOI MOSFET and partial SOI type isolation MOSFETs having silicon film thickness of 15nm. The buried insulators having different dielectric constant were used, including SiO2(k=3.9), Si3N4(k=7.5), HfO2(k=25). Vd,sat is 1.6[V] and Vd,lin is 0.1[V]

Figure 5 shows the I_{ds}-V_{gs} characteristic for V_{ds}=1.6[V]. Since the buried insulator partially removes the drain doped region, the transconductance of the partial SOI type isolation MOSFET is slightly reduced. However, since the source region which is the source of most electrons, is maintained, the transconductance is not significantly reduced compared to planar MOSFETs.

Also, Fig. 6 shows the drain current as a function of drain voltage for the different buried insulator materials. Since the partial SOI type isolation MOSFET has a small depletion region width near the drain region, the phenomenon of channel length modulation is minimized. Therefore, a saturation current slope with the gentle slope appears in the structure having SiO_2(k=3.9) as the buried insulator.

And Fig. 7 shows DIBL characteristics according to gate channel length. As the gate channel length becomes shorter, the DIBL of the planar MOSFET deteriorates sharply. On the other hand, the partial SOI type isolation MOSFET having buried insulator of a low dielectric constant has a gentle slope due to small depletion region width near drain region.

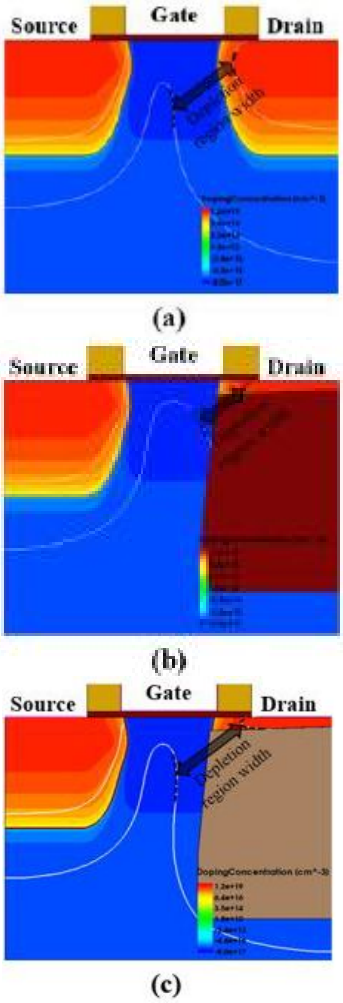


Fig 4. Two-dimensional cross-sectional view of planar MOSFET and partial SOI type isolation MOSFETs having different dielectric constant and its doping profile. The white lines of the view are Depletion region. There are the arrows for depletion region with near drain region in (a) planar MOSFET, (b) SiO2(k=3.9) and (c) HfO2(k=25). The silicon film Thickness of the devices is 15nm respectively. Vgs is 0[V], and Vds is 1.6[V]

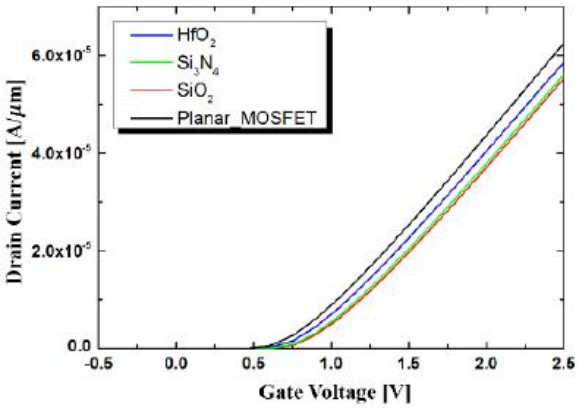


Fig 5. Ids-Vgs characteristic for planar MOSFET and partial SOI type isolation MOSFETs. Vds is 1.6[V]. The silicon film thickness of partial SOI type isolation MOSFET is 15nm respectively.

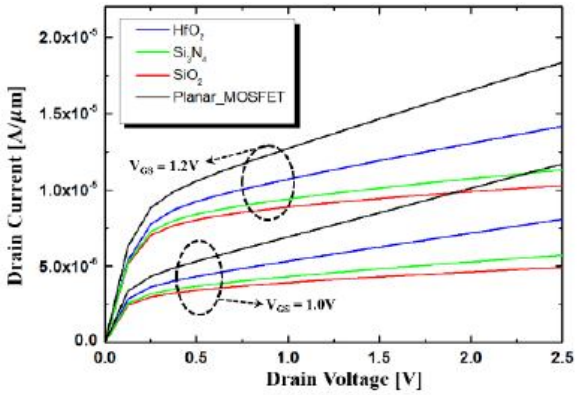


Fig 6. Id-Vds characteristic for planar MOSFET and partial SOI type isolation MOSFETs. The silicon film thickness of partial SOI type isolation MOSFET is 15nm respectively.

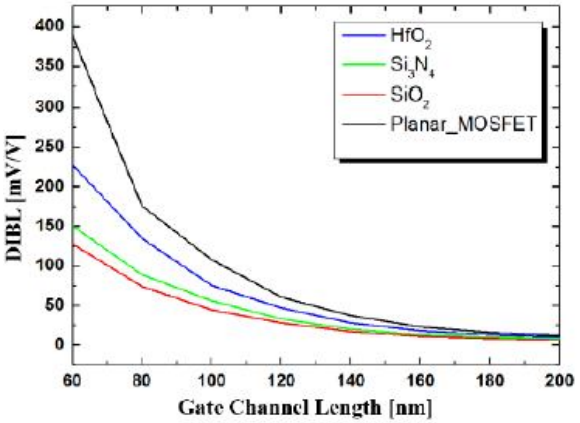


Fig 7. DIBL characteristic according to the gate channel length for planar MOSFET and partial SOI type isolation MOSFETs

CONCLUSION

From the simulation analysis of a partial SOI type isolation MOSFET, we found that the depletion region width decrease near the drain region. It is an important part of improving DIBL and V_{th}

characteristics. We have analyzed the characteristics of the device by using various dielectric constants of the buried insulator and confirmed that it will play an important role in improving the characteristics of the DRAM cell.

REFERENCES

[1] Lee, Myoung Jin, Jun Hee Cho, Sang Don Lee, Jin Hong Ahn, Jin Woong Kim, Sung Wook Park, Y.j. Park, and Hong Shick Min. "Partial SOI Type Isolation for Improvement of DRAM Cell Transistor Characteristics." IEEE Electron Device Letters, vol.26, no.5, 2005.

[2] Young Kwon Kim, Jin Sung Lee, Geon Kim, Taesik Park, Hui Jung Kim, Young Pyo Cho, Young June Park, and Myoung Jin Lee, "The optimized Partial Insulator Isolation MOSFET(PiFET)," Journal of Semiconductor Technology and Science, vol.17, no.5, 2017.

[3] M. Jagadesh Kumar, Senior Member and Anurag Chaudhry, "Two-Dimensional Analytical Modeling of Fully Depleted DMG SOI MOSFET and Evidence for Diminished SCEs," IEEE transactions on electron devices, vol.51, no.4, (2004).

[4] Anurag Chaudhry and M. Jagadesh Kumar, "Investigation of the Novel Attributes of a Fully Depleted Dual-Material Gate SOI MOSFET," IEEE transactions on electron devices, vol.51, no.9, 2004.

[5] Anurag Chaudhry and M. Jagadesh Kumar, "Controlling Short-Channel Effects in Deep-Submicron SOI MOSFETs for Improved Reliability: A Review," IEEE transactions on electron devices, vol.4, no.1, 2004.

[6] Wu-Shiung Feng, T. Y. Chan and Chenming Hu, "MOSFET Drain Breakdown Voltage," IEEE transactions on electron devices, vol.7, no.7, 1986.

[7] J. Chen, T. Y. Chan, I. C. Chen, P. K. Ko and Chenming Hu, "Subbreakdown Drain Leakage Current in MOSFET," IEEE electron device letters, vol.8, no.11 1987.

[8] SURYA VEERARAGHAVAN and JERRY G. FOSSUM, "Short-Channel Effects in SO1 MOSFET's," IEEE transactions on electron devices, vol.36, no.3, (1989).

[9] J. P. Colinge, "Reduction of kink effect in thin-film SOI MOSFET's," IEEE Electron Device Lett., vol. 9, pp. 97–99, Feb. 1988.

★★★