A COMPACT LOW-VOLTAGE ANALOG CMOS EXPONENTIAL FUNCTION GENERATOR

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Abstract: A compact and low-voltage analog CMOS exponential function generator which operates with a single power supply voltage is designed in 0.18µm CMOS standard technology. The proposed circuit uses a current input voltage divider in order to perform the pseudo approximation to implement the exponential function generator. Simulation results using HSPICE shows more than 15 dB output voltage range while the error less than ±0.5dB .The total power consumption is below 0.2 mW with a single 1.5 V power supply.

Keywords: CMOS analog integrated circuit, Exponential function generator, pseudo exponential, High-Accurate, Low-voltage circuit.

I. INTRODUCTION

The exponential function generator is essential and important building block in a variable gain amplifier (VGA) [I].However, unlike the BJT device, there is no intrinsic logarithmic device working in saturation for CMOS technologies. For overcoming this problem pseudo- approximations is used widely in the previously reported literature.[1]-[9] To implement the exponential function by this method, different approximations have been already introduced; Taylor series second order [2]–[5], Taylor series fourth order [6], pseudo-exponential [7], pseudo-Taylor approximation [8], modified pseudo Taylor approximation [9], which in all of them MOSFET are operating in the strong inversion region.

However, the reported circuits aren't well suited for low-voltage operations. Moreover, most of reported circuits use two power supply voltages (±1.5 V) while by downscaling of CMOS process, analog circuits have been forced to operate with continually decreasing supply voltage. Another method for implementing the exponential function in CMOS technology is using MOSFET in the weak inversion region [10] However, the poor matching, limited bandwidth, and modest dynamic range of these devices have forced the employment of the quasi-quadratic law of MOS transistors in strong inversion and saturation.

This paper proposes a compact and low-voltage exponential function generator. The proposed circuit provides more than 15 dB range with the linearity error less than ± 0.5 dB, while consumes extremely low power (less than 0.2 mW) at low-voltage applications (The circuit uses a single 1.5 power supply). Moreover, the proposed circuit offers controllable output voltage by adjusting the bias current. This feature isvery useful for analog and mixed-mode circuits such as VGAs and AGCs.

In section 2, proposed exponential function generator is explained. Error analysis is accomplished in section 3 and simulation results are presented in section 4.Finally, conclusion is made in Section 5.

II. CIRCUIT DESCRIPTION

The pseudo-exponential approximation which is used in this paper is given [7]

$$f(x) = \frac{1+0.5x}{1-0.5x} \cong exp(x) \qquad if\ |x| < 1 \qquad (1)$$

The comparison between the pseudo-exponential function and exp(x) is shown in Fig. 1. The Fig.1 shows that as x varies from -0.85 to 0.85, the output dynamic range can be more than 15 dB while the difference between f(x) and exp(x) is less than ± 0.5 dB.

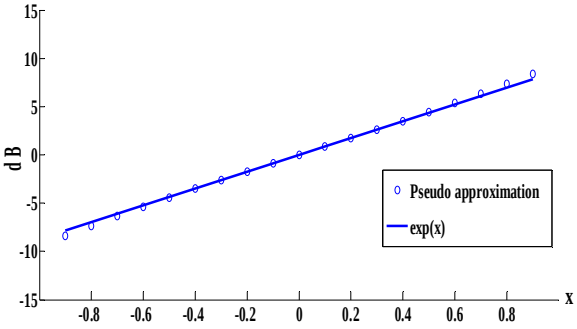


Fig.1. Comparison between exp(x) and pseudo approximation method

The proposed low-voltage exponential function generator is illustrated in Fig.2

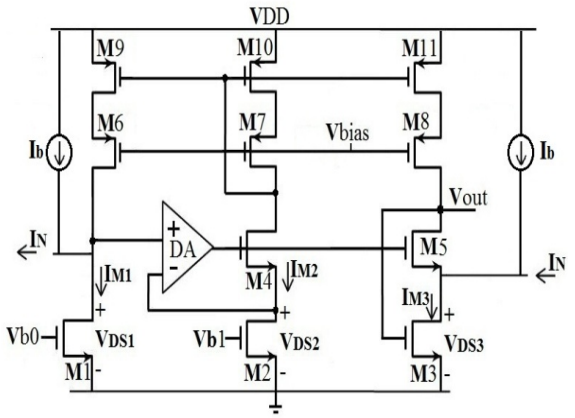


Fig.2. The proposed current-input/ voltage-output exponential function generator

Assume that transistors M1, M2 and M3 are biased to operate in triode region.
The differential amplifier (DA) and transistor M4 establish a negative feedback loop in order to fix the drain-source voltage of M1 and M2 at the same value.

$$V_{DS1} = V_{DS2} \qquad (2)$$

The differential amplifier circuit is sketched in Fig.3
The choice of the PMOS differential pair rests on the fact that the input voltage which is sensed by the differential amplifier is small. Moreover, a capacitor CComp is needed at the gate of Md5 in order to compensate the feedback loop.[11]
In addition, the drain-source voltage of transistors M2 and M3 are matched thanks to transistor M4 and M5, that the gate-source voltages of these transistors are identical.

$$V_{DS2} = V_{DS3} \qquad (3)$$

The above equation is guaranteed by the upper PMOS current mirrors M7, M8, M10 and M11 which replicate the current IM2 to the right branch. Since the source voltage of M4 and M5 are equal, i.e., VSB4=VSB5 and Vth3=Vth4 therefore the assumption that VGS3=VGS4 could be held.

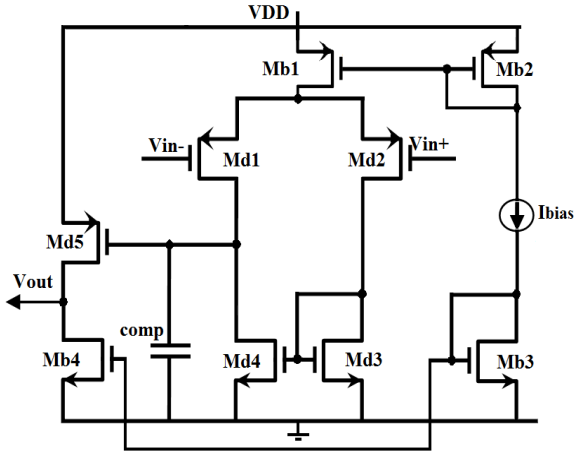


Fig.3. Differential amplifier

Equation (2) and (3) lead to:

$$V_{DS1} = V_{DS2} = V_{DS3} = V_{DS} \qquad (4)$$

Neglecting body effect the drain current of transistors M1, M2 and M3 are given by

$$I_{M1} = K_1\left[(V_{b0} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad (5)$$

$$I_{M2} = K_2\left[(V_{b1} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad (6)$$

$$I_{M3} = K_3\left[(V_{out} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad (7)$$

Where $K_1=K_2=K_3=K=\mu C_{ox}\frac{W}{L}$ and Vth is the threshold voltage of M1, M2 and M3.
The drain current of M1 is the sum of Ib-IN and the mirrored drain current of M1 and can be expressed as

$$I_b - I_N + I_{M2} = I_{M1} \qquad (8)$$

Assume that M1, M2 and M3 are perfectly matched ($K_1=K_2=K_3=k$) and by substituting equation (5) and (6) into equation (8), Ib-IN is derived as

$$I_b - I_N = k(V_{b0} - V_{b1})V_{DS} \qquad (9)$$

The drain current of M3 is also given by

$$I_{M3} = I_N + I_b + I_{M2} \qquad (10)$$

By replacing equation (6) and (7) into equation (10) the IN+Ib is derived as

$$I_N + I_b = k(V_{out} - V_{b1})V_{DS} \qquad (11)$$

Thus, by substituting equation (9) into (11) the Vout yields

$$V_{out} - V_{b1} = (V_{b0} - V_{b1})\frac{I_b + I_N}{I_b - I_N} \qquad (12)$$

$$V_{out} - V_{b1} = (V_{b0} - V_{b1})\frac{1+\frac{I_N}{I_b}}{1-\frac{I_N}{I_b}} \cong (V_{b0} - V_{b1})\exp\left(2\frac{I_N}{I_b}\right) \qquad (13)$$

Consequently, if Vout is referred to Vb1, an exponential function generator is obtained. The output swing of the proposed circuit is defined by the difference (Vb0-Vb1) and is independent of the variation of supply voltage which it is an advantage in compare with previously reported circuit.[1]
In order to the proposed exponential function generator works properly, M1 and M2 and M3 have to work in triode region and other transistors should be in saturation. So, the current IN must flow into the drain of M3 and should be:

$$I_N < K(V_{b0} - V_{th1})(V_{b0} - V_{b1}) + I_b \qquad (14)$$

Where k is transcoductance of transistors M1, M2 and M3 and Vth1 is the threshold voltage of M1 respectively.

ERROR ANALYSIS

In this section, two kinds of systematic errors will be discussed; mobility reduction and transistor mismatch.

3.1. Mobility Reduction Error:

Mobility reduction is the main source of systematic error in the proposed circuit. Since the division is done by means of transistors which operating in triode region and these transistors have different gate voltages, the mobility reduction is likely to impair the performance of the proposed circuit.
Considering Θ the mobility reduction coefficient, equation (5),(6) and (7) will modified as follow:[11]-[13]

$$I_1 = \frac{K}{1+\theta(V_{b0}-V_{th})}\left[(V_{b0}-V_{th})V_{DS}-\frac{1}{2}V_{DS}^2\right] \quad (15)$$

$$I_2 = \frac{K}{1+\theta(V_{b1}-V_{th})}\left[(V_{b1}-V_{th})V_{DS}-\frac{1}{2}V_{DS}^2\right] \quad (16)$$

$$I_3 = \frac{K}{1+\theta(V_{out}-V_{th})}\left[(V_{out}-V_{th})V_{DS}\frac{1}{2}V_{DS}^2\right] \quad (17)$$

By introducing in the above equations the first Taylor approximation of the denominators and after some manipulation the following approximation equation for the divider output will be obtained.

$$V_{out}-V_{b1} = (V_{b0}-V_{b1})exp\left(2\frac{I_N}{I_b}\right)(1+\varepsilon_\theta) \quad (18)$$

Where ε_θ is the mobility reduction error and equal to:

$$\varepsilon_\theta \cong \theta(V_{b0}-V_{b1})\left(\frac{I_b}{I_N-I_b}\right) \quad (19)$$

Equation (19) shows the error is proportional to the coefficient Θ and also to (Vb0-Vb1). Since the output voltage of the proposed circuit is also dependent to this difference (Vb0-Vb1), a trade off between accuracy and output range appears.

3.2. Mismatch error:

While the mismatch between the transistors of same type can be minimized by careful layout, we defined the mismatch among M1, M2 and M3 as $\Delta k_1=K_1-K$, $\Delta k_3=K_3-K$
Where K is transconductance of transistor M2 and K1, K3 are transconductance of transistor M1 and M3 respectively.
Considering these mismatches the equation (5),(6) and (7) will be modified as follow:

$$I_2 = K\left[(V_{b1}-V_{th})V_{DS}-\frac{1}{2}V_{DS}^2\right] \quad (20)$$

$$I_1 = (K+\Delta K_1)\left[(V_{b0}-V_{th})V_{DS}-\frac{1}{2}V_{DS}^2\right] \quad (21)$$

$$I_3 = (K+\Delta K_3)\left[(V_{out}-V_{th})V_{DS}-\frac{1}{2}V_{DS}^2\right] \quad (22)$$

For $\left(\frac{\Delta K_3}{k}\right)^2 \ll 1$ and $\left(\frac{\Delta K_1}{k}\right)^2 \ll 1$ and after some manipulation, it can be shown that

$$V_{out}-V_{b1}-\varepsilon_1 = (V_{b0}-V_{b1}+\varepsilon_2)\exp\left(2\frac{I_N}{I_b}\right) \quad (23)$$

Where $\varepsilon_1 = \frac{\Delta K_3}{k}(V_{b1}-V_{th})$ and $\varepsilon_2 = \frac{\Delta K_1}{k}(V_{b0}-V_{th})-\frac{\Delta K_3}{k}(V_{b1}+V_{b0})$

Equation (23) implies that the output voltage of the exponential function generator is equal to exponential of the current IN/Ibwith a gain factor and constant DC voltage which is different from equation (12), so the mismatch only cause change of gain and position in DC characteristic.

SIMULATION RESULTS

The proposed exponential function generator was laid out in standard 0.18µm CMOS technology.
The minimum supply voltage is limited by the path formed by M10, M7 , M4 and M2 so the minimum supply voltage is

$$V_{DD}^{Min} = V_{GSM10}+V_{DS4}+V_{DS2} \quad (24)$$

Where VGSM10 is gate-source voltage of M10 , VDS4 is the minimum voltage drop in transistor M4 and can be as small as 0.15V in 0.18µm CMOS technology and VDS2 is the drain-source voltage of M2 which is depended to input currents. So, VDD=1.5 V is selected in order to have an appreciable voltage swing.
Post layout simulations from extracted circuit using HSPICE and level 49 parameters (BSIM3V3) for the proposed circuit is shown in Fig.4. With the reference current Ib =25 µA, when IN varies from -30 to 15 µA, the Output dynamic range could be more than 15 dB while the linearity error is within ±0.5 dB and the power dissipation is less than 0.2 mW.
The error between the output of the proposed circuit and ideal exponential function (exp (2IN/Ib)) is limited between -0.5 to 0.5 dB when -30 µA< IN < 15 µA, as shown in Fig.5

CONCLUSIONS

A low-voltage high-accurate CMOS analog exponential function generator has been introduced. The proposed circuit operates with a single 1.5 V power supply and shows more than 15 dB of

amplitude variation with the error less than ±0.5 dB. (The input current varies from -30 µA to 15 µA with the error less than ±0.5 dB). The power dissipation is below 0.2 mW. Consequently, the proposed exponential function generator has potential to be employed in modern high-performance low-voltage VGA and analog signal processing systems.

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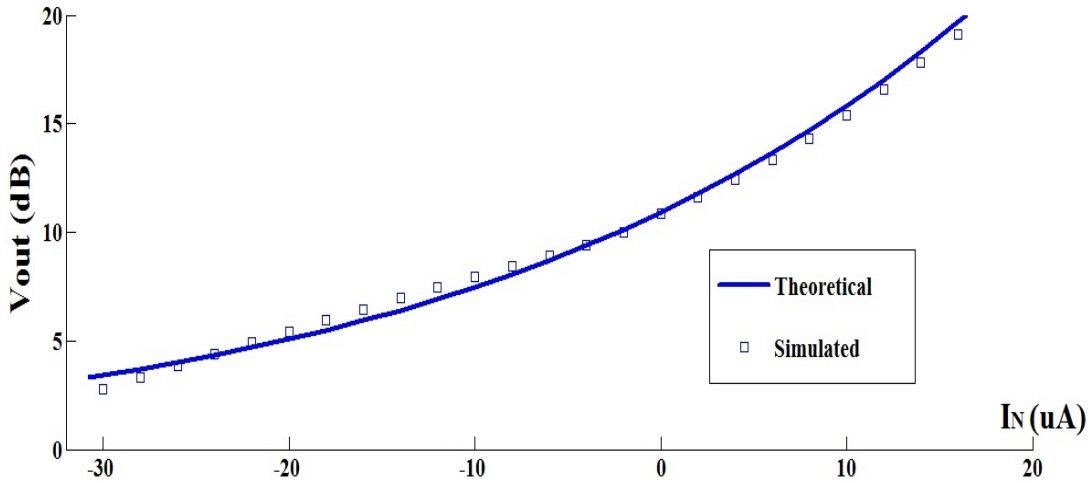


Fig.4.Simulation result of the proposed exponential function generator

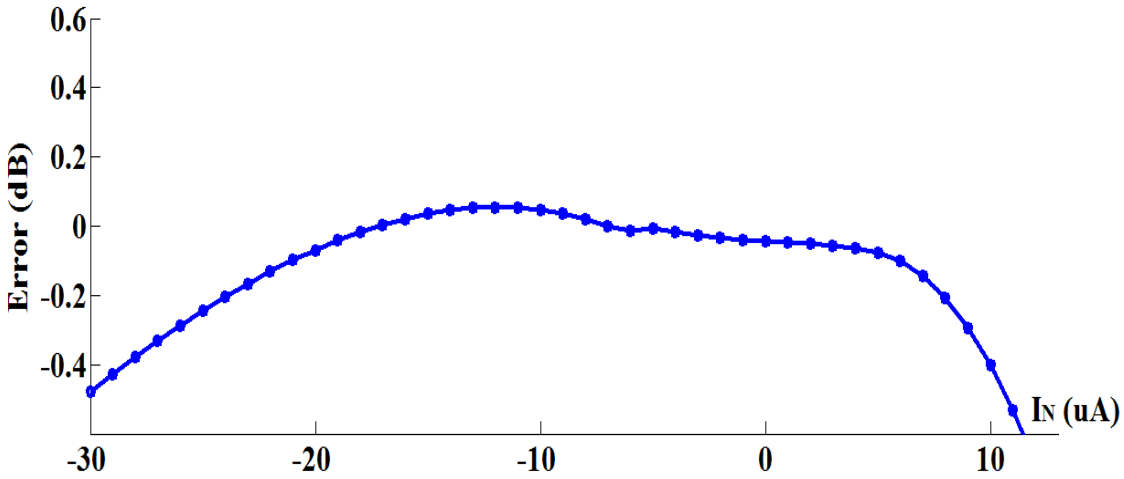


Fig.5. Error in dB scale