D LATCH FLIP FLOP USING SPATIAL WAVE FUNCTION SWITCHED FIELD-EFFECT TRANSISTORS

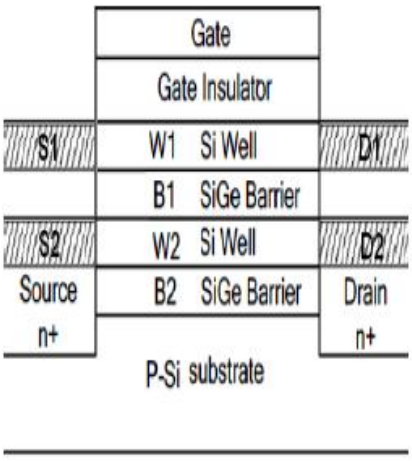
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Abstract- This paper aims at designing D-Latch circuits that are 25% smaller in size by using high-mobility n-channel spatial wavefunction switching SWSFETs which provide significant reduction of cell area and power dissipation. SWS-FETs comprise of vertically stacked quantum well/quantum dot channels allowing the drain current flow in multiple channels in a single transistor1. A two quantum channel SWS-FET structure comprises of two Si quantum wells sandwiched between SiGe barriers (as shown in Fig. 1). The fabrication process of SWS-FETs is compatible with conventional complementary metal-oxide-semiconductor (CMOS) FETs2. This device allows the drain current flow in multiple channels in a single transistor (Fig. 2 shows the IDS-VGS characteristics of a two well single SWS-FET).

D Latches find applications including shift register, one bit delay and memories. It has 4 NAND gates with each gate having 4 transistors "2 n-MOS and 2 p-MOS". The two inputs signal the data and the clock control the output Q. When the clock "Ck" is high, the Q output follows any changes from data "D", and when the clock "Ck" is low, the Q is latched and the Q output will not change states even when data changes. The SWS-NAND logic gates can be realized using three n-SWS-FET3 as shown in Fig. 3, and Fig 4 shows the simulation result.

In this work four SWS-NAND gates are used to perform D Latch function, the Figure 5 presents the schematic circuit of the D Latch flip flop and the comparison between SWS and CMOS D Latch shows in figure 6, the conventional CMOS circuit has 16 transistors" 8-pmos and 8-nmos" , but the SWS has only 12-n channel SWS FET transistors. Where CMOS process parameters is 0.35µm and SWS model is based on integration between Berkeley Short-channel IGFET Model (BSIM) and Analog Behavioral Model.



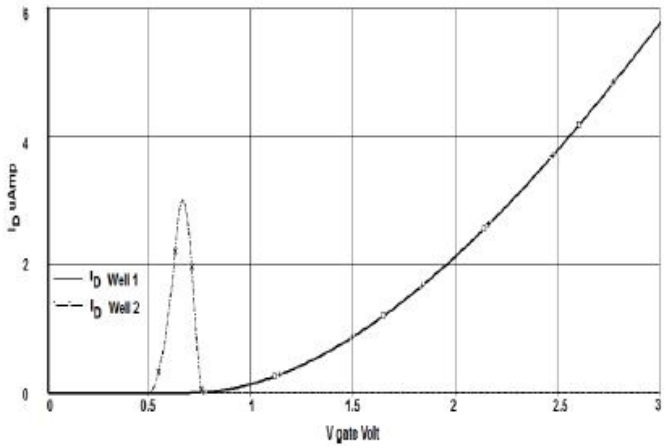
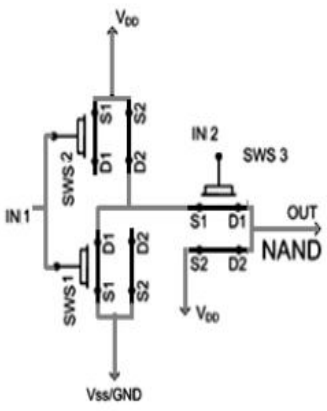
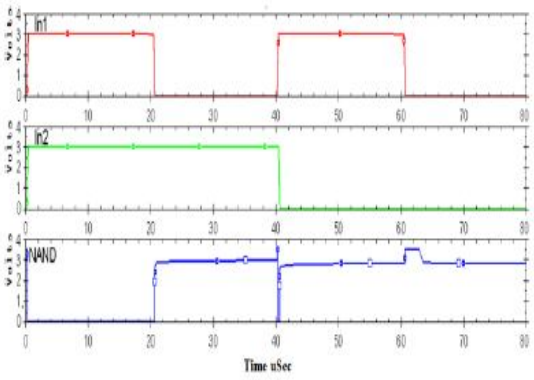


Figure 1. The two channel SWS-FET structure Figure 2. SWS-FET IDS-VGS Characteristics





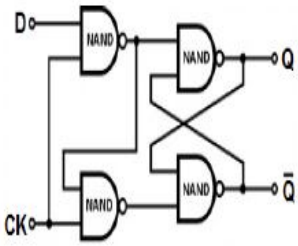


Figure 3. Two input SWS NAND Figure 4. The simulation of n-channel SWS NAND Figure 5. The D Latch

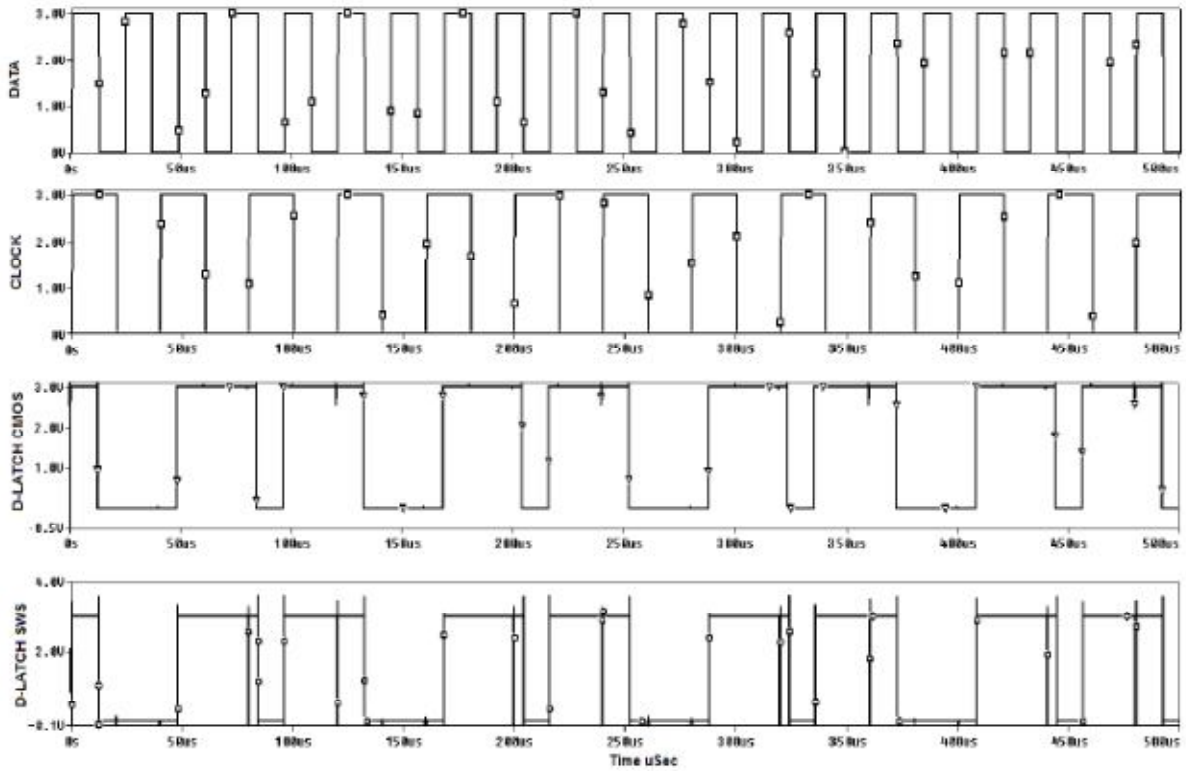


Figure 5. Figure 4. The simulation of D Latch circuit

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